VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please amend the specification as follows:

Page 39, please replace paragraph [0130] with the following replacement paragraph:

--The die pad 901 is expanded at every side to form bonding area 917 for power supply. The semiconductor package further includes a plate 913 of high dielectric constant material provided on the die pad 901. On the plate 913, a metal plate 919 is formed. The high dielectric constant material 913 may be ceramics, such as alumina (aluminum oxide) and titan oxide. The plate 913 may be adhered between the die pad 901 and metal plate 919. The die pad 901 is bent by about 0.1 to 0.3 mm around a chip mounting area 920 so that the inner leads 905 becomes higher in level than the chip mounting area 920. The metal plate 919 is shaped to be slightly (0.5 to 1.0 mm) [small] smaller than the die pad 901.--

IN THE CLAIMS:

Please cancel claims 47 and 54 without prejudice or disclaimer to the subject matter recited therein.

Please amend the claims as follows:

46. (Twice Amended) A semiconductor apparatus, comprising:

a substrate;

a die pad which comprises a power supply bonding area which is formed by extending outwardly all the sides of the die pad;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

first conductive patterns which are formed on the substrate and are connected to the ground terminals;

second conductive patterns which are formed on the substrate and are connected to the power supply terminals and the power supply bonding area;

a high dielectric constant layer formed on the die pad; and

a metal layer formed on the high dielectric constant layer and having a chip mounting area on which a semiconductor chip is mountable and a ground bonding area surrounding the chip mounting area, the ground bonding area being connected to the first conductive patterns, wherein the metal layer is provided with a ridge completely surrounding the chip mounting area so as to define the chip mounting area and ground bonding area.

50. (Amended) A semiconductor apparatus according to claim 46, wherein the [metal layer is provided with a] ridge [surrounding the chip mounting area so as to] separates the chip mounting area from the ground bonding area.

53. (Amended) A ball grid array semiconductor package, comprising:

an substrate;

a die pad which is formed on an upper surface of the substrate, and which comprises a power supply bonding area which is formed by extending outwardly all the sides of the die pad;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

first conductive patterns which are formed on the upper surface of the substrate and are connected to the ground terminals;

second conductive patterns which are formed on the upper surface of the substrate and are connected to the power supply terminals and the power supply bonding area;

a high dielectric constant layer formed on the die pad;

a metal layer formed on the high dielectric constant layer and having a chip mounting area on which a semiconductor chip is mountable and a ground bonding area surrounding the chip mounting area, the ground bonding area being connected to the first conductive patterns, the metal layer being provided with a ridge that completely surrounds the chip mounting area so as to define the chip mounting area and ground bonding area;

ball mounting pads disposed on a lower surface of the substrate;

interconnecting patterns which electrically couple the first and second conductive patterns to respective ones of the ball mounting pads; and

solder balls mounted on the ball mounting pads.

55. (Amended) A ball grid array semiconductor package according to claim [58] 53, wherein the high dielectric constant layer is composed of ceramics.

56. (Amended) A ball grid array semiconductor package according to claim [58] 55, wherein the high dielectric constant [material] layer is alumina (aluminum oxide) and titan oxide.

57. (Amended) A ball grid array semiconductor package according to claim [58] 53, wherein the [metal layer is provided with a] ridge [surrounding the chip mounting area so as to] separates the chip mounting area from the ground bonding area.

58. (Amended) A ball grid array semiconductor package according to claim [58] 53, wherein the metal layer has a shape that is smaller than a shape of the die pad.

59. (Amended) A ball grid array semiconductor package according to claim [63] 58, wherein the metal layer partially covers the die pad, and wherein the power supply bonding area is a part of the die pad that is not covered by the metal layer.